REMARKS

Applicants appreciate the Examiner's thorough examination of the subject application and request reconsideration of the subject application based on the foregoing amendments and the following remarks.

Claims 1-34, 36 and 37 are pending in the subject application. Claims 2-13, 16-17, 19-22, 24-34, 36 and 37 are acknowledged as being allowable by the Examiner.

Claims 1, 14-15, 18 and 23 stand rejected under 35 U.S.C. §102.

Claim 14 was amended in the instant amendment for clarity so as to more distinctly claim Applicant's invention. The amendments to the claims are supported by the originally filed disclosure.

35 U.S.C. §102 REJECTIONS

The Examiner rejected claims 1, 14-15, 18 and 23 under 35 U.S.C. §102(e) as being anticipated by Yanagi, et al. [USP 6,359,607; "Yanagi"]. Applicants respectfully traverse as discussed below. Because claims were amended in the instant amendment, the following discussion refers to the language of the amended claims. However, only those amended features specifically relied upon to distinguish the claimed invention from the cited prior art shall be considered as being made to overcome the cited reference. The following separately addresses the rejection as to claim 1, claims 14-15, and claims 18 and 23.

CLAIM 1

Claim 1 stands rejected as being anticipated by Yanagi for the reasons provided on pages 2-3 of the above referenced Office Action. In particular, the Office Action indicates that Yanagi discloses *inter alia* controlling a voltage applied to the pixel electrodes (pixel potential Vdp as shown in figure 12, col. 2, lines 30-32 thereof) in a conduction period of the pixel switching elements (scanning voltage Vgh applied to a gate electrode, TFT attains an ON state (see col. 2, lines 23-29)) according to a pulse width supplied to the signal lines. It is further indicated that Yanagi discloses that the voltage being applied to the pixel electrodes is less than a voltage supplied to the signal lines (pixel potential Vdp is less than potential Vsp by a level shift ΔVdp as shown in figure 12 thereof), and that the voltage applied to the signal line is determined to be higher than a desired charging voltage required for the pixel electrodes so that the voltage applied to the pixel electrodes becomes a desired voltage (desired voltage Vdp). Applicants respectfully traverse and also respectfully disagree with the characterization of what is allegedly disclosed in Yanagi.

Applicants claim, claim 1, a method for driving an image display device which includes a plurality of pixel electrodes which are formed on a substrate, pixel switching elements which are individually connected to the pixel electrodes, a plurality of signal lines for applying a data signal according to a display image to the pixel electrodes, and a common electrode for applying a common potential to pixels. The method controls a voltage applied to the pixel electrodes in a conduction period of the pixel switching elements according to a pulse width supplied to the signal lines. Also, in the conduction period of the pixel switching elements, the voltage applied

to the pixel electrodes is less than a voltage supplied to the signal lines, and the voltage applied to the signal lines is determined to be higher than a desired charging voltage required for the pixel electrodes so that the voltage applied to the pixel electrodes becomes a desired value.

As the Examiner has admitted; the methodology of the present invention as set forth in claim 1 is directed to the voltage being applied to the pixel electrodes *in or during the conduction period of the pixel switching elements* and not during the period following the conduction period when the switching elements are turned OFF. As is known to those skilled in the art, and as alos described in Yanagi and the subject application, the pixel switching elements are switched ON and OFF by the scanning lines, more particularly the voltage being supplied to the swirching elements over the scanning lines. As is also known to those skilled in the art, the transistor of a three-terminal element is drawn toward the negative side by the parasitic capacitance between a gate and a drain when the scanning line is switched from ON to OFF.

As disclosed in Yanagi, and as admitted by the Examiner, when a scanning voltage Vg of potential Vgh is applied from the scanning signal line driving circuit 300 to a gate electrode of a TFT of one display pixel as shown in figure 12, the TFT attains an ON state. Yanagi also discloses (see col. 2, lines 50-60 and figure 12), that when the scanning voltage Vg falls from the ON potential Vgh to a low-level voltage Vgl, this voltage corresponds to an OFF state of the TFT (e.g., see col. 1, lines 55-61, col. 2, lines 50-55). In other words, when the scanning line voltage Vg drops to Vgl, the switching element is turned OFF and thus is not in a conducting state.

In the grounds for the rejection, the Examiner refers to the disclosure and discussion in Yanagi that does not relate to the operational period when the TFT is in the ON state but rather

refers to the discussion and disclosure that is applicable when the TFT is on the OFF state. It is clear from the discussion in col. 2, line 50-col. 3, line 2 and col. 4, lines 12-26 of Yanagi, as well as related discussion in the subject application, the level shift (ΔVdp) the Examiner is referring to in support of the specific grounds of rejection, namely that the voltage being applied to the pixel electrodes is less than the signal line voltage Vsp, is in fact that which occurs as a consequence of the parasitic capacitance and at the falling of the scanning voltage Vg from Vgh to Vgl. This also is abundantly clear from the relationship provided in col. 2, line 60 of Yanagi, which shows that this level shift is proportional to the difference between Vgh and Vgl.

As such, it is clear from figure 12 of Yanagi that the voltage being applied to the pixel electrodes when the switching element (i.e., the TFT) is the potential or voltage of the signal line (i.e., Vsp), whereby the liquid crystal material comprising the pixel is charged to a desired potential. It should be remembered that the waveform being depicted in figure 12 of Yanagi as Vd necessarily represents the potential of the liquid crystal material as it is being charged when a voltage is applied across the pixel electrodes. Also, it is clear that in Yanagi when the switching element is turned OFF (i.e., by the falling scanning line voltage, Vg) a level shift is seen in the potential of the pixel (Vd) due to the described parasitic capacitance shift described in Yanagi as well as the subject application. It should be noted that Vd is described in Yanagi as being the drain waveform (see col. 2, lines 11-15) however, Yanagi also refers elsewhere that Vd is the pixel potential (see col. 2, lines 55-60).

In addition Applicants would note that in the present invention a higher voltage is supplied to the signal line than is required for the pixel electrode, so as to write a desired voltage

to the pixel electrode. On the other hand, Yanagi, as described in col. 4, line 65 to col. 5, line 21 thereof, is directed to lowering of the level shift ΔVd of the pixel electrode by controlling the scan signal so that the signal does not fall abruptly. Yanagi does not indicate the technical concept of the present invention. Yanagi, as in Fig. 12, lowers the voltage supply Vdp to the pixel electrode to a level below the desired voltage by causing a level shift ΔVd, whereby the pixel potential is drawn toward the negative side, when the scan line switches from ON to OFF, instead of setting the voltage supply to the signal line to Vsp which is greater than Vdp so as to write the voltage Vdp to the pixel electrode.

Applicants also would note that Yanagi nowhere includes a discussion like that found on pages 31-36 of the subject application detailing the shortcomings of the conventional practice as well as attributes that flow from the methodology of the present invention and the advantageous effects this would have on reducing power consumption.

In sum, Yanagi does not anywhere disclose a method for driving an image display device as is set forth in claim 1 including, *inter alia*:

(1) controlling a voltage being applied to the pixel electrodes in a conduction period of the pixel switching elements according to a pulse width supplied to the signal lines,

(2) where the voltage being applied to the pixel electrodes in the conduction period of the pixel switching elements, is less than a voltage supplied to the signal lines, and

(3) the voltage being applied to the signal lines is determined to be higher than a desired charging voltage required for the pixel electrodes so that the voltage applied to the pixel electrodes becomes a desired value.

It is respectfully submitted that claim 1 is patentable over the cited reference for the foregoing reasons.

CLAIMS 14-15

Claims 14 and 15 stand rejected as being anticipated by Yanagi for the reasons provided on pages 3-4 of the above referenced Office Action. Applicants respectfully traverse. Claim 14 was amended in the foregoing amendment as suggested by the Examiner to more particularly describe that the negative voltages and positive voltages being applied to the pixels is separately controlled so as to be adaptable to the alternating polarity of the applied voltage to the pixel.

Applicants claim, claim 14, a method for driving an image display device, including displaying tones by modulating a pulse width of a two-value voltage supplied to signal lines and where a polarity of a voltage applied to pixels is changed for each scanning line, and in voltage application to pixel electrodes with a reference voltage 0V, an amplitude of scanning lines is varied between positive application for applying a voltage to a positive side and negative application for applying a voltage to a negative side. Also, the voltage being applied on the positive side and negative side are controlled based on differences in charging characteristics for negative and positive voltages.

As indicated in the subject application, the characteristics of the switching elements vary depending on the polarity of the voltage (e.g., see Figs 1-2 thereof). As also indicated in the subject application (e.g., see page 19 and 63), with the pulse-width modulating driving technique, tones are expressed by stopping charging of pixels during charging.

As indicated previously by Applicants Yanagi only teaches or discloses that the scanning pulse includes an intermediate ON region (linear region) between a threshold level VT of the TFT and the level Vgh (see column 3, lines 38-49 thereof). Further, figure 13 and the description thereof in Yanagi provides no teaching or disclosure regarding the polarity at the application. Thus, and in contrast to Figures 39-41 of the subject application, Yanagi does not teach nor disclose that the amplitude of the signal line varies per vertical period, adapting to the alternating polarity of the applied voltage to the pixel per scanning line, in other words, the amplitudes of the signal lines are different between the positive application and the negative application. It thus necessarily follows that Yanagi cannot disclose or teach the methodology as claimed by Applicants. This is not disclosed anywhere in Yanagi.

Applicants also would note, with reference to in Figs. 39-41 and page 65, lines 17-25 of the subject application, that the present invention changes the amplitude on the scan line for every vertical period, that is, it changes the amplitude on the scan line when writing a signal of a positive value and a signal of a negative value, so that the scan line voltage is lower when writing a negative voltage than when writing a positive voltage. In contrast, in Fig. 12 of Yanagi, Vgh and Vgl are a gate on voltage and a gate off voltage, and TF1 and TF2 share the same Vgp-p (i.e., Vgh-Vgl). The cited reference therefore by no means can disclose, teach or suggest the methodology as set forth in claim 14.

As to claim 15, this claim adds the further limitations that a difference in amplitude of a voltage supplied to the scanning lines is equal to an amplitude of a voltage supplied to a common electrode. As indicated in the subject application (e.g., see page 66 thereof) when the difference

in amplitude between the positive and negative voltage applications are equal to the amplitude of the common voltage; this makes it unnecessary to provide an additional elements for creating the difference.

It is respectfully submitted that claims 14 and 15 are patentable over the cited reference for the foregoing reasons.

CLAIMS 18, 23

Claims 18 and 23 stand rejected as being anticipated by Yanagi for the reasons provided on pages 4-5 of the above referenced Office Action. Applicants respectfully traverse.

Applicants claim, claim 18, a driving device of an image display device which includes a plurality of pixel electrodes which are formed on a substrate, pixel switching elements which are individually connected to the pixel electrodes, a plurality of signal lines for applying a data signal according to a display image to the pixel electrodes, and a common electrode for applying a common potential to pixels. The driving device applies a voltage between a potential of the signal lines and a potential of the common electrode when a potential of scanning lines is ON, and displaying tones by modulating a pulse width of a two-value voltage supplied to the signal lines. The driving device also includes a signal line driving section for supplying a voltage, not less than a voltage supplied to the pixel electrodes, to the signal lines so that the voltage applied to the pixel electrodes becomes a voltage taking into account change of an optimum counter voltage according to a display tone.

The Office Action asserts that Yanagi discloses a signal line driving section for supplying a voltage not less than a voltage supplied to the pixel electrodes (asserted that Vsp is greater than Vd in figure 12, to the signal lines so that the voltage applied to the pixel electrodes becomes a voltage taking into account change of an optimum counter voltage according to a display tone. Applicants respectfully disagree.

Applicants also would note that, as also provided in the discussion regarding claim 1, Yanagi cannot disclose nor describe a driving section that supplies a voltage to the signal lines that is not less than a voltage supplied to the pixel electrodes. As indicated above in the discussion regarding claim 1, Yanagi discloses that the voltage being applied to the pixel electrodes when the switching element is in the ON state is the potential or voltage of the signal line, Vsp. As such, it necessarily follows that Yanagi cannot disclose supplying a voltage to the signal lines when the switching element is in the ON state that can be greater than the voltage being applied to the pixel electrodes.

As also indicated above in the discussion regarding claim 1, in the present invention a higher voltage is supplied to the signal line than is required for the pixel electrode, so as to write a desired voltage to the pixel electrode. On the other hand, Yanagi, as described in col. 4, line 65 to col. 5, line 21 thereof, is directed to lowering of the level shift ΔVd of the pixel electrode by controlling the scan signal so that the signal does not fall abruptly. Yanagi, as in Fig. 12, lowers the voltage supply Vdp to the pixel electrode to a level below the desired voltage by causing a level shift ΔVd, whereby the pixel potential is drawn toward the negative side, when the scan line

switches from ON to OFF, instead of setting the voltage supply to the signal line to Vsp which is greater than Vdp so as to write the voltage Vdp to the pixel electrode.

The Office Action also asserts that Yanagi discloses applying a voltage between a potential of the signal lines and a potential of the common electrode when a potential of the scanning lines is ON and displaying tones by modulating a pulse width of a two-value voltage supplied to the signal line. As to the modulating pulse width, the Office Action refers to voltage Vs applied to the signal lines as shown in figure 12 of Yanagi. Applicants respectfully disagree that Yanagi discloses this. It should be noted that Yanagi merely provides (see col. 1, line 60-col. 2, line 4) that with the described operation for turning the switching elements ON and OFF using the scanning lines, image signals outputted from the signal line driving circuit 200 to the respective signal lines 104 are written in respective corresponding pixels.

It is respectfully submitted that the foregoing remarks distinguishing claim 18 from the cited reference also applies to distinguish the image display device of claim 23 from the cited reference.

It is respectfully submitted that claims 18 and 23 are patentable over the cited reference for the foregoing reasons.

The following additional remarks shall apply to each of the above.

As the Federal Circuit has indicated, in deciding the issue of anticipation, the trier of fact must identify the elements of the claims, determine their meaning in light of the specification and prosecution history, and identify *corresponding elements* disclosed in the allegedly anticipating

reference (emphasis added, citations in support omitted). *Lindemann Maschinenfabrik GMBM v. American Hoist and Derrick Company et al.*, 730 F. 2d 1452, 221 USPQ 481,485 (Fed. Cir. 1984). In concluding that the '770 Patent did not anticipate the claims, the Federal Circuit in *Lindemann Maschinenfabrik GMBM v. American Hoist and Derrick Company et al.*, at 221 USPQ 485-486, further provides that:

> The '770 patent discloses an entirely different device, composed of parts distinct from those of the claimed invention, and operating in a different way to process different materials differently. Thus, there is no possible question of anticipation by equivalents. Citations omitted.

It is clear from the foregoing remarks, that the allegedly corresponding elements disclosed in Yanagi do not in fact correspond to the elements of the claimed invention. It also is clear that the devices described in Yanagi function and operate in a different manner from that of the claimed invention. As also indicated above, the method disclosed and taught in Yanagi for driving an image device is different from that claimed and taught by Applicants. Thus, there can be no disclosure or teaching in Yanagi of Applicants' invention.

As provided in MPEP-2131, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Or stated another way, "The identical invention must be shown in as complete detail as is contained in the ... claims. *Richardson v Suziki Motor Co.*, 868 F.2d 1226, 9 USPQ 2d. 1913, 1920 (Fed.

Cir. 1989). Although identify of terminology is not required, the elements must be arranged as required by the claim. *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990). It is clear from the foregoing remarks that the above identified claims are not anticipated by the cited reference.

It is respectfully submitted that for the foregoing reasons, claims 1, 14-15, 18 and 23 are patentable over the cited reference and satisfy the requirements of 35 U.S.C. §102(e). As such, these claims are allowable.

It is respectfully submitted that the subject application is in a condition for allowance. Early and favorable action is requested.

Applicants believe that additional fees are not required for consideration of the within Response. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, the Commissioner is hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,
Edwards & Angell, LLP

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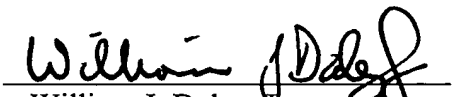
By: 

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